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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,863	01/10/2001	Toyohiko Yoshida	49657-921	6032

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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	09/756,863	YOSHIDA, TOYOHIKO
	Examiner	Art Unit
	Aimee J. Li	2183

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 December 2006</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-12,14,16,18 and 19</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-12,14,16,18 and 19</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12, 14, 16, and 18-19 have been considered.

2. In view of the Appeal Brief filed on 11 December 2006, PROSECUTION IS HEREBY REOPENED. The rejection is set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

4. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6.   Claims 1-5, 12, 14, 16, and 18-19 are rejected under 35 U.S.C. 102(a) as being taught by

Soni, European Patent Application EP 1 006 438 A1 (herein referred to as Soni).

7.   Referring to claims 1 and 12, taking claim 12 as exemplary, Soni has taught an

instruction memory attached with a translator, used with a processor configured to execute

instructions in a first instruction architecture as a native instruction, comprising:

      a.   An instruction storage unit to store an instruction in a second instruction

architecture (Soni paragraph 0034 "…the microprocessor instruction is fetched

from instruction cache 40 and placed in instruction streaming buffer 53…" and

Figure 3); and

      b.   An instruction translator to translate an instruction in said second instruction

architecture output from said instruction storage unit into an instruction in said

first instruction architecture for application to said processor, wherein said

processor is configured to execute instructions only in said first instruction

architecture (Soni paragraph 0009 "…a microprocessor to fetch and decode that

instruction into associated RISC micro-operations and store the micro-ops…";

paragraph 0035 "…between on and three instructions are submitted to decoders

45, 46, 47 for translation into micro-ops…"; and Figure 3);

      c.   Said instruction translator including:

            i.   A translator to read out the instruction in said second instruction

architecture from said instruction storage unit in response to a received

first address of an instruction to be executed by said processor (Soni

paragraph 0049 "…Also, shown is address and comparison logic 102…"

and Figure 4) and translate the read out instruction in said second

instruction architecture into the instruction in said first instruction

architecture (Soni paragraph 0009 "...a microprocessor to fetch and

decode that instruction into associated RISC micro-operations and store

the micro-ops..."; paragraph 0035 "...between on and three instructions

are submitted to decoders 45, 46, 47 for translation into micro-ops..."; and

Figure 3);

ii.   An instruction cache to temporarily hold the instruction in said first

instruction architecture after the translation by said translator in

association with the first address (Soni paragraph 0037 "...The decoded

instruction queue can hold up to six (6) micro-ops..."; paragraph 0040

"...Decoded instruction queue 49 is interconnected to parcel cache 52

such that decoded instructions (parcels) can be loaded from queue 49 into

parcel cache 52..."; and Figure 3); and

iii.   A selector to search said instruction cache in response to a received second

address of an instruction to be executed by said processor and selectively

output to said processor (Soni paragraph 0011 "...The parcel cache is

coupled to the microprocessor fetch/decode unit and can be searched

during an instruction fetch cycle..."; paragraph 0049 "...Address

translation and comparison logic 102 includes a translation lookaside

buffer (TLB) that translates the 32 bit linear address into a 36-bit physical

memory address..."; paragraph 0055 "...parcel cache 52 includes address

translation and compare logic 112 similar to logic 102 and 107 in the

instruction cache and BTB, respectively. This will allow the parcel cache

to be looked up (searched)…"; and Figure 4), based on a determination

result of whether or not an instruction corresponding to the instruction of

the address is held in said instruction cache, an instruction output by said

translator or the corresponding instruction in said first instruction

architecture held in said instruction cache (Soni paragraph 0011 "…When

a parcel(s) corresponding to the complex microprocessor instruction being

fetched is found in the parcel cache a hit occurs and the corresponding

micro-ops are then provided to the execution units…"; paragraph 0035-

0039 "…After RAT/ROB unit 51 the micro-ops are provided to

reservation station 50 and sent to the execution units for processing…";

paragraph 0040 "…When a 'hit' occurs on the parcel cache 52, the parcel

is then provided to reservation station 50…"; and Figure 3).

8.   Claim 1 has similar limitations to claim 12 and is rejected for similar reasons.

9.   Referring to claim 2, Soni has taught the instruction translator according to claim 1,

wherein said second instruction architecture is a variable length instruction architecture, and said

translator includes a variable length translator for translating an instruction in said second

instruction architecture read out from said instruction memory into one or more instructions in

said first instruction architecture, the number of which depends on an instruction length of the

read out instruction in said second instruction architecture (Soni paragraph 0004 "…instructions

in the Intel ISA are complex…" and paragraphs 0007-0009 …a microprocessor to be able to

fetch a complex instruction and decode that instruction into associated RISC micro-operations

and store the micro-ops…").

10.   Referring to claim 3, Soni has taught the instruction translator according to claim 2,

wherein said variable length translator translates the instruction in said second instruction

architecture read out from said instruction memory into an instruction in said first instruction

architecture having a total length depending on and larger than the instruction length of said read

out instruction in said second instruction architecture (Soni paragraphs 0035-0036 "…decoder 0

is a complex decoder that can decode any instruction not greater than seven bytes and that

translates into no more than four micro-ops…Some instructions translate into more than four

micro-ops…" and Figure 3).

11.   Referring to claim 4, Soni has taught the instruction translator according to claim 3,

wherein each instruction in said first instruction architecture includes one or a plurality of sub

instructions, and the number of the sub instructions included in the instruction in the first

instruction architecture translated by said variable length translator depends on the instruction

length of said read out instruction in said second instruction architecture (Soni paragraphs 0035-

0036 "…decoder 0 is a complex decoder that can decode any instruction not greater than seven

bytes and that translates into no more than four micro-ops…Some instructions translate into

more than four micro-ops…" and Figure 3).

12.   Referring to claim 5, Soni has taught the instruction translator according to claim 1,

wherein said translator includes a plurality of translators which translate a plurality of

instructions in said second instruction architecture read out from said instruction memory into

one instruction in said first instruction architecture (Soni paragraphs 0035-0036 "…decoder 0 is

a complex decoder that can decode any instruction not greater than seven bytes and that

translates into no more than four micro-ops...Some instructions translate into more than four

micro-ops..." and Figure 3).

13.   Referring to claim 14, Soni has taught the instruction memory attached with a translator

according to claim 12, further comprising an address translator to translate an address at the time

of reading from said instruction storage unit (Soni paragraph 0049 "...Also, shown is address

and comparison logic 102..." and Figure 4).

14.   Referring to claim 16, Soni has taught a data processing apparatus, comprising:

    a.   A processor operating with an instruction in a first instruction architecture as a

           native instruction (Soni paragraph 0004 "...instructions in the Intel ISA are

           complex..." and paragraphs 0007-0009 ...a microprocessor to be able to fetch a

           complex instruction and decode that instruction into associated RISC micro-

           operations and store the micro-ops...");

    b.   A bus to which said processor is connected (Soni paragraph 0013 "...A central

           processing unit (CPU) 10...is provided and interconnected to the various

           components by system bus 12..."; Figure 1; and Figure 3 – In regards to Soni,

           there are multiple buses within the system. The first bus is bus 12 shown in

           Figure 1, which is the external bus connecting the CPU to all peripherals. The

           other buses are found within CPU 10 connecting all the elements within CPU 10

           and are show by the arrowed lines in Figure 3.);

    c.   A first instruction memory (Soni paragraph 0034 "...the microprocessor

           instruction is fetched from instruction cache 40 and placed in instruction

streaming buffer 53...” and Figure 3) with a translator interconnected with said

processor through said bus (Soni paragraph 0009 “...a microprocessor to fetch

and decode that instruction into associated RISC micro-operations and store the

micro-ops...”; paragraph 0035 “...between on and three instructions are

submitted to decoders 45, 46, 47 for translation into micro-ops...”; and Figure 3);

and

d.   A second instruction memory interconnected to said processor through said bus

(Soni paragraph 0037 “...The decoded instruction queue can hold up to six (6)

micro-ops...”; paragraph 0040 “...Decoded instruction queue 49 is interconnected

to parcel cache 52 such that decoded instructions (parcels) can be loaded from

queue 49 into parcel cache 52...”; and Figure 3), said first instruction memory

with a translator including:

i.   A first instruction storage unit to store an instruction in a second

instruction architecture transferred from said processor through said bus

(Soni paragraph 0034 “...the microprocessor instruction is fetched from

instruction cache 40 and placed in instruction streaming buffer 53...” and

Figure 3); and

ii.   An instruction translator to translate the instruction in said second

instruction architecture output from said first instruction storage unit into

an instruction in said first instruction architecture for application to said

processor through said bus (Soni paragraph 0049 “...Also, shown is

address and comparison logic 102...” and Figure 4) and translate the read

out instruction in said second instruction architecture into the instruction

in said first instruction architecture (Soni paragraph 0009 "...a

microprocessor to fetch and decode that instruction into associated RISC

micro-operations and store the micro-ops..."; paragraph 0035 "...between

on and three instructions are submitted to decoders 45, 46, 47 for

translation into micro-ops..."; and Figure 3), and

iii.   Said second instruction memory including:

    (1)   A second instruction storage unit to store an instruction in said first

instruction architecture transferred from said processor through

said bus (Soni paragraph 0037 "...The decoded instruction queue

can hold up to six (6) micro-ops..."; paragraph 0040 "...Decoded

instruction queue 49 is interconnected to parcel cache 52 such that

decoded instructions (parcels) can be loaded from queue 49 into

parcel cache 52..."; and Figure 3); and

    (2)   An instruction reading circuit responsive to an address signal

applied from said processor through said bus for applying an

instruction in said first instruction architecture output from said

second instruction storage unit to said processor through said bus

(Soni paragraph 0011 "...The parcel cache is coupled to the

microprocessor fetch/decode unit and can be searched during an

instruction fetch cycle..."; paragraph 0049 "...Address translation

and comparison logic 102 includes a translation lookaside buffer

(TLB) that translates the 32 bit linear address into a 36-bit physical

memory address..."; paragraph 0055 "...parcel cache 52 includes

address translation and compare logic 112 similar to logic 102 and

107 in the instruction cache and BTB, respectively. This will

allow the parcel cache to be looked up (searched)..."; and Figure

4).

15.   Referring to claim 18, Soni has taught the data processing apparatus according to claim

16, wherein the number of clock cycles spent by said processor to access said first instruction

memory through said bus is larger than the number of clock cycles spent by said processor to

access said second instruction memory through said bus (Soni paragraph 0004 "...Hence, the

complexity of x86 instructions puts a large burden on the front end of the processor pipeline with

respect to logic complexity, timing and number of pipeline stages..."; paragraph 0011 "...In this

manner, the present invention improves performance by minimizing the amount of hardware

resources (i.e. fetch/decode logic) utilized while maintaining compatibility..."; and Figure 3).

16.   Referring to claim 19, Soni has taught the data processing apparatus according to claim

16, further comprising a third instruction memory with a translator interconnected to said

processor through said bus, said third instruction memory with a translator including:

        a.   A third instruction storage unit to store an instruction in a third instruction

               architecture different from said second instruction architecture, said instruction in

               said third instruction architecture being transferred from said processor through

               said bus (Soni paragraph 0037 "...The decoded instruction queue can hold up to

               six (6) micro-ops..."; paragraph 0040 "...Decoded instruction queue 49 is

interconnected to parcel cache 52 such that decoded instructions (parcels) can be loaded from queue 49 into parcel cache 52...", and Figure 3); and

    b.   An instruction translation circuit responsive to an address signal applied from said processor through said bus, for translating an instruction in said third instruction architecture output from said third instruction storage unit into an instruction in said first instruction architecture for application to said processor (Soni paragraph 0011 "...The parcel cache is coupled to the microprocessor fetch/decode unit and can be searched during an instruction fetch cycle..."; paragraph 0049 "...Address translation and comparison logic 102 includes a translation lookaside buffer (TLB) that translates the 32 bit linear address into a 36-bit physical memory address..."; paragraph 0055 "...parcel cache 52 includes address translation and compare logic 112 similar to logic 102 and 107 in the instruction cache and BTB, respectively. This will allow the parcel cache to be looked up (searched)..."; and Figure 4).

Claim Rejections - 35 USC § 103

17.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18.   Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni, European Patent Application EP 1 006 438 A1 (herein referred to as Soni) as applied to claim 1

above, and further in view of Goettelmann et al., U.S. Patent No. 5,313,614 (herein referred to as

Goettelmann).

19.   Regarding claim 6, Soni has not explicitly taught wherein:

   a.   Each instruction in said first instruction architecture can include one or a plurality

         of sub instructions,

   b.   Said translator translates a plurality of instructions in said second instruction

         architecture read out from said instruction memory into an instruction in said first

         instruction architecture including sub instructions, the number of which depends

         on the number of said plurality of instructions.

20.   Goettelmann has taught the translation from a source instruction architecture

(Goettelmann, "source machine code" of Fig.11) into a native instruction architecture

(Goettelmann, "translated code" of Fig.11), wherein the native architecture contains a plurality

of sub-instructions (Goettelmann, "expanded intermediate language code" of Fig.11), sub-

instructions which can then be removed if necessary in order to reduce the translated code size

(Goettelmann, Col.4 lines 6-18). One of ordinary skill in the art would have recognized that it is

desirable to reduce the size of instruction code so that less hardware (memory space) is needed,

thus lowering costs. Therefore, one of ordinary skill in the art would have found it obvious to

modify the instruction translator of Soni to further translate instructions from a source

architecture into a native architecture that includes a plurality of sub-instructions in order to

reduce the amount of instruction storage required to store the translated code. Furthermore,

because the number of native instructions are dependent on the length of the varying-length

source instruction as shown above, and because the number of sub instructions depend on the

native instructions, then the number of sub-instructions depend on the length of the source

instructions.

21.   Regarding claim 7, Soni in further view of Goettelmann have taught wherein the number

of sub instructions included in the instruction in said first instruction architecture after said

translation is equal to the number of said plurality of instructions (see Goettelmann "BEQ Label

instruction" of "source machine code", its corresponding "BFALSE FlagZ, Label" instruction of

"translated code", with associated sub-instruction "BFALS.d FlagZ, Label" of "expanded

intermediate language code", all of Fig.11).

22.   Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni,

European Patent Application EP 1 006 438 A1 (herein referred to as Soni) as applied to claim 1

above, and further in view of Gregor, U.S. Patent No. 5,023, 776 (herein referred to as Gregor).

23.   Referring to claim 8, Soni has taught The instruction translator according to claim 1,

wherein said translator translates said read out instruction in said second instruction architecture

into one or a plurality of instructions as the instruction in said first instruction architecture (Soni

paragraphs 0035-0036 "...decoder 0 is a complex decoder that can decode any instruction not

greater than seven bytes and that translates into no more than four micro-ops...Some instructions

translate into more than four micro-ops..." and Figure 3). Soni has not taught said instruction

translator further comprises a controller for controlling said instruction cache so that said

instruction cache holds each of said one or said plurality of instruction held in said instruction

cache as an entry which can be invalidated in one of first and second conditions. Gregor has

taught the holding of a cache line within a cache so that it cannot be replaced until an EOP signal

is detected in order to reduce cache busy time and improve processor performance (Gregor,

Col.22 lines 36-67). One of ordinary skill in the art would have recognized that it is desirable, as

well as a main goal of microprocessor design, to improve the performance of a microprocessor.

Therefore, one of ordinary skill in the art would have found it obvious to modify the cache of

Emma in view of IBM to hold a plurality of instructions in a cache until an EOP signal is

detected. Furthermore, because the claim language is in the alternative format, only one of the

two invalidation condition requirements is required to be met, and thus the EOP signal that is

detected (Gregor, Col.22 lines 56-57) can be considered such a signal.

24.   Referring to claim 10, Soni in further view of Gregor has taught wherein said controller

outputs a signal asserted when a new instruction cannot be held in said instruction cache without

invalidating an entry which can be invalidated in the second condition (Gregor, Col.22 lines 36-

67).

25.   Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soni,

European Patent Application EP 1 006 438 A1 (herein referred to as Soni), in further view of

Gregor, U.S. Patent No. 5,023, 776 (herein referred to as Gregor), as applied to claim 8 above,

and further in view of Schacham et al., U.K. Patent Application GB220481A (herein referred to

as Schacham).

26.   Referring to claim 9, Soni in further view of Gregor has taught wherein said first

condition is a holding control condition by hardware control based on a prescribed algorithm by

said instruction cache (Gregor, Col.22 lines 36-67). Soni in further view of Gregor has not

taught wherein the said second condition is a condition in which an explicit invalidation

instruction is applied from the outside of said instruction cache. However, in the parent claim of

claim 9, only one of the two invalidation conditions must be met. Therefore, because Soni in

further view of Gregor has satisfied one of the conditions, namely the holding control condition

as shown above, the claim language is satisfied. Furthermore, even though the alternative form

claim language is met, Schacham has taught that a cache invalidation instruction can be executed

to invalidate the entire instruction cache or a portion of it (Schacham, p.4 lines 28-30) in order to

maintain proper cache coherence and provide better processor performance (Schacham, p.2 lines

8-23).. One of ordinary skill in the art would have recognized that it is desirable, as well as a

main goal of microprocessor design, to improve the performance of a microprocessor.

Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction

cache of Soni in further view of Gregor to allow a cache invalidation instruction to be executed

so that cache coherency is maintained and processor performance is improved.

27.   Referring to claim 11, Soni in further view of Gregor has taught the instruction translator

according to claim 8, wherein said translator translates the read out instruction in said second

instruction architecture into the plurality of instructions as the instruction in said first instruction

architecture (Soni paragraphs 0035-0036 "...decoder 0 is a complex decoder that can decode any

instruction not greater than seven bytes and that translates into no more than four micro-

ops...Some instructions translate into more than four micro-ops..." and Figure 3). Soni in

further view of Gregor has not taught said controller provides said first condition with one of

said plurality of instructions and said second condition with each of said plurality of instructions

but said one instruction. Schacham has taught that a cache invalidation instruction can be

executed to invalidate the entire instruction cache or a portion of it (Schacham, p.4 lines 28-30)

in order to maintain proper cache coherence and provide better processor performance

(Schacham, p.2 lines 8-23). One of ordinary skill in the art would have recognized that it is

desirable, as well as a main goal of microprocessor design, to improve the performance of a

microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to

modify the instruction cache of Soni in further view of Gregor to allow a cache invalidation

instruction to be executed so that cache coherency is maintained and processor performance is

improved. Furthermore, Soni in further view of Gregor in view of Schacham has taught the

invalidation of instructions in a cache based upon one of two conditions, namely a holding

control condition as taught by Gregor, and a cache invalidation instruction as taught by

Schacham. One of ordinary skill in the art would have recognized that because some instructions

will have the first condition associated with them, and others will have the second condition

associated with them. Therefore, one of ordinary skill in the art would have found it obvious that

the processor of Soni in further view of Gregor further in view of Schacham will provide one

instruction with a first condition, and other instructions with a second condition.

Response to Arguments

28.   Applicant's arguments, see Appeal Brief, filed 11 December 2006, with respect to the

rejection(s) of claim(s) 1-12, 14, 16, and 18-19 have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new

ground(s) of rejection is made in view of the above rejection.

Conclusion

29.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

      a.   Soni, U.S. Patent Number 6,223,254, is the related U.S. Patent to the European

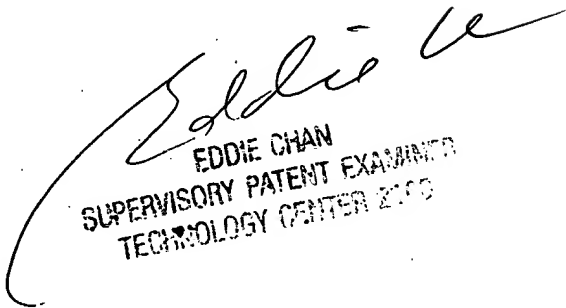   Patent used in the above rejection.

30.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The

examiner can normally be reached on M-T 7:00am-4:30pm.

31.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

32.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

                                        Aimee J Li
                                        Examiner
                                        Art Unit 2183

15 April 2007

                                        EDDIE CHAN
                                        SUPERVISORY PATENT EXAMINER
                                        TECHNOLOGY CENTER 2100